LINFINITY
MICROELECTRONICS

REGULATING PULSE WIDTH MODULATOR

DESCRIPTION

This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power applications. The SG1524 is specified for operation over the full military ambient temperature range of -55°C to +125°C, the SG2524 for -25°C to +85°C, and the SG3524 is designed for commercial applications of 0°C to +70°C.

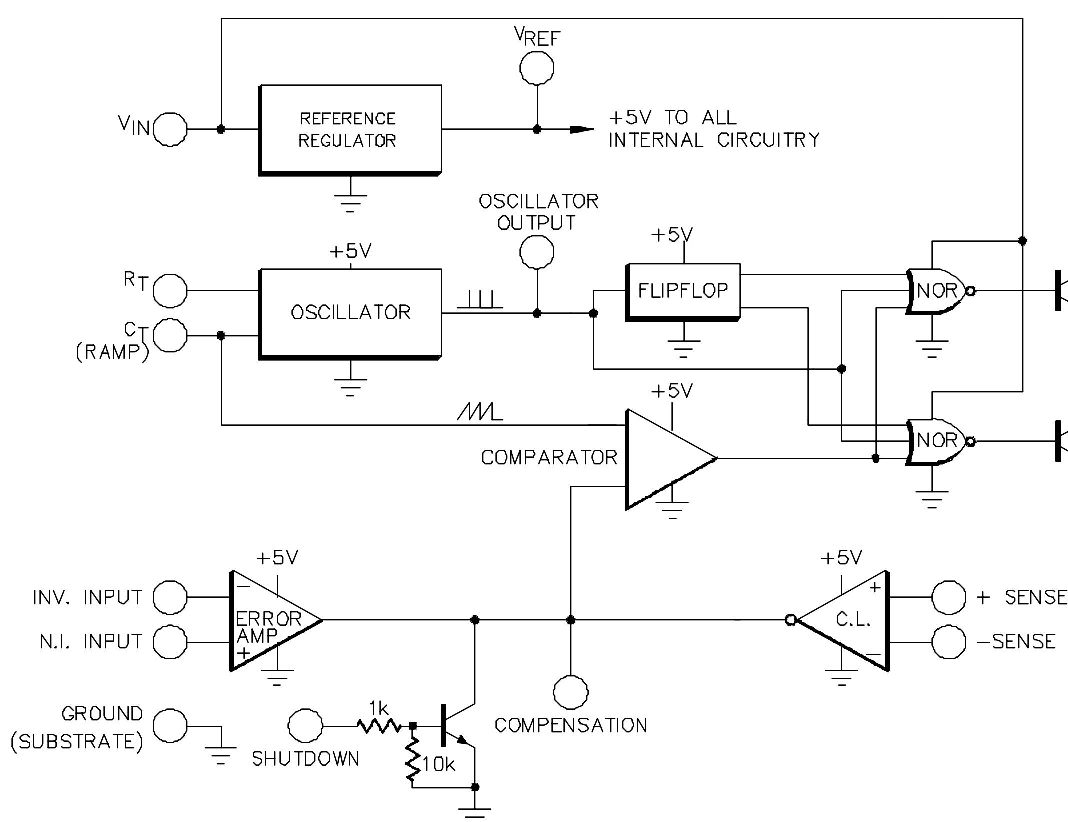
FEATURES

- **8V to 40V operation**
- **5V reference**
- **Reference line and load regulation of 0.4%**
- **Reference temperature coefficient < ± 1%**
- **100Hz to 300KHz oscillator range**
- **Excellent external sync capability**
- **Dual 50mA output transistors**
- **Current limit circuitry**
- **Complete PWM power control circuitry**
- **Single ended or push-pull outputs**
- **Total supply current less than 10mA**

HIGH RELIABILITY FEATURES - SG1524

- ♦ **Available to MIL-STD-883B and DESC SMD**
- ♦ **MIL-M-38510/12601BEA - JAN1524J**
- ♦ **Radiation data available**
- ♦ **LMI level "S" processing available**

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage (+V_{IN}) 42V
Collector Voltage 40V
Logic Inputs .... -0.3V to 5.5V
Current Limit Sense Inputs .... -0.3V to 0.3V
Output Current (each transistor) 100mA
Reference Load Current 50mA
Oscillator Charging Current 5mA
Operating Junction Temperature
  Hermetic (J, L Packages) .... 150°C
  Plastic (N, D Packages) .... 150°C
Storage Temperature Range .... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) .... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DATA

J Package:
  Thermal Resistance-Junction to Case, θ_{JC} .... 30°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} .... 80°C/W
N Package:
  Thermal Resistance-Junction to Case, θ_{JC} .... 40°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} .... 65°C/W
D Package:
  Thermal Resistance-Junction to Case, θ_{JC} .... 50°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} .... 120°C/W
L Package:
  Thermal Resistance-Junction to Case, θ_{JC} .... 35°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} .... 120°C/W

Note A. Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
Note B. The above numbers for θ_{JC} are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θ_{JA} numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage (+V_{IN}) .... 8V to 40V
Collector Voltage .... 0V to 40V
Error Amp Common Mode Range .... 1.8V to 3.4V
Current Limit Sense Common Mode Range .... -0.3V to 0.3V
Output Current (each transistor) .... 0 to 50mA
Reference Load Current .... 0 to 20mA
Oscillator Charging Current .... 30µA to 2mA
Oscillator Frequency Range .... 100Hz to 300KHz
Oscillator Timing Resistor (R_T) .... 1.8KΩ to 100KΩ
Oscillator Timing Capacitor (C_T) .... 1nF to 1.0µF
Operating Ambient Temperature Range
  SG1524 .... -55°C to 125°C
  SG2524 .... -25°C to 85°C
  SG3524 .... 0°C to 70°C

Note 2: Range over which the device is functional and parameter limits are guaranteed.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1524 with -55°C ≤ T_A ≤ 125°C, SG2524 with -25°C ≤ T_A ≤ 85°C, SG3524 with 0°C ≤ T_A ≤ 70°C, and +V_{IN} = 20V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1524/2524			SG3524			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section (Note 3)								
Output Voltage	T_J = 25°C	4.80	5.00	5.20	4.60	5.00	5.40	V
Line Regulation	V_{IN} = 8V to 40V			20			30	mV
Load Regulation	I_L = 0 to 20mA			50			50	mV
Temperature Stability (Note 7)	Over Operating Temperature Range			50			50	mV
Total Output Voltage Range (Note 7)	Over Line, Load and Temperature	4.80		5.20	4.60		5.40	V
Short Circuit Current	V_{REF} = 0V	25	50	150	25	50	150	mA

Note 3. I_L = 0mA

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ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	SG1524/2524			SG3524			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillator Section (Note 4)								
Initial Accuracy	T_J = 25°C	36	40	44	36	40	44	KHz
	MIN ≤ T_J ≤ MAX	34		46	34		46	KHz
Voltage Stability	V_{IN} = 8V to 40V		0.1	1		0.1	1	%
Maximum Frequency	R_T = 2KΩ, C_T = 1nF	200	400		200	400		KHz
Sawtooth Peak Voltage	V_{IN} = 40V	3		3.8	3		3.8	V
Sawtooth Valley Voltage	V_{IN} = 8V	0.6	1	1.2	0.6	1	1.2	V
Clock Amplitude		3.2			3.2			V
Clock Pulse Width		0.3		1.5	0.3		1.5	µs
Error Amplifier Section (Note 5)								
Input Offset Voltage	R_S ≤ 2KΩ		0.5	5		2	10	mV
Input Bias Current			1	10		1	10	µA
Input Offset Current				1			2	µA
DC Open Loop Gain	R_L ≥10MΩ, T_J = 25°C	72			60			dB
Output Low Level	$V_{PIN 1}$ - $V_{PIN 2}$ ≥ 150mV		0.2	0.5		0.2	0.5	V
Output High Level	$V_{PIN 2}$ - $V_{PIN 1}$ ≥150mV	3.8	4.2		3.8	4.2		V
Common Mode Rejection	V_{CM} = 1.8V to 3.4V	70						dB
Supply Voltage Rejection	V_{IN} = 8V to 40V	55						dB
Gain-Bandwidth Product (Note 7)	T_J = 25°C	1	2		1	2		MHz
P.W.M. Comparator (Note 4)								
Minimum Duty Cycle	V_{COMP} = 0.5V			0			0	%
Maximum Duty Cycle	V_{COMP} = 3.6V	45	49		45	49		%
Current Limit Amplifier Section (Note 6)								
Sense Voltage	T_J = 25°C	190	200	210	180	200	220	mV
Input Bias Current				200			200	µA
Shutdown Section								
Threshold Voltage	T_J = 25°C	0.5	0.8	1.2	0.5	0.8	1.2	V
	MIN ≤ T_J ≤ MAX	0.2		1.8	0.2		1.8	V
Output Section (each transistor)								
Collector Leakage Current	V_{CE} = 40V			50			50	µA
Collector Saturation Voltage	I_C = 50mA			2			2	V
Emitter Output Voltage	I_E = 50mA	17			17			V
Collector Voltage Rise Time	R_C = 2KΩ			0.4			0.4	µs
Collector Voltage Fall Time	R_C = 2KΩ			0.2			0.2	µs
Power Consumption								
Standby Current	V_{IN} = 40V		7	10		7	10	mA

Note 4. F_{OSC} = 40KHz (R_T = 2.9KΩ, C_T = .01µF)
Note 5. V_{CM} = 2.5V
Note 6. V_{CM} = 0V
Note 7. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

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APPLICATION NOTES

OSCILLATOR

The oscillator in the SG1524 uses an external resistor R_T to establish a constant charging current into an external capacitor C_T. While this uses more current than a series-connected RC, it provides a linear ramp voltage at C_T which is used as a time-dependent reference for the PWM comparator. The charging current is equal to $3.6V/R_T$, and should be restricted to between 30µA and 2mA. The equivalent range for R_T is 1.8K to 100K.

The range of values for C_T also has limits, as the discharge time of C_T determines the pulse width of the oscillator output pulse. The pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output deadtime relationship is shown in Figure 1. A pulse width below 0.35 microseconds may cause failure of the internal flip-flop to toggle. This restricts the minimum value of C_T to 1000pF. (Note: Although the oscillator output is a convenient oscilloscope sync input, the probe capacitance will increase the pulse width and decrease the oscillator frequency slightly.) Obviously, the upper limit to the pulse width is determined by the modulation range required in the power supply at the chosen switching frequency. Practical values of C_T fall between 1000pF and 0.1µF, although successful 120 Hz oscillators have been implemented with values up to 5µF and a series surge limit resistor of 100 ohms.

The oscillator frequency is approximately $1/R_T \bullet C_T$; where R is in ohms, C is in microfarads, and the frequency is in Megahertz. For greater accuracy, the chart in Figure 2 may be used for a wide range of operating frequencies.

Note that for buck regulator topologies, the two outputs can be wire-ORed for an effective 0-90% duty cycle range. With this connection, the output frequency is the same as the oscillator frequency. For push-pull applications, the outputs are used separately; the flip-flop limits the duty cycle range at each output to 0-45%, and the effective switching frequency at the transformer is 1/2 the oscillator frequency.

If it is desired to synchronize the SG1524 to an external clock, a positive pulse may be applied to the clock pin. The oscillator should be programmed with R_T and C_T values that cause it to free-run at 90% of the external sync frequency. A sync pulse with a maximum logic 0 of +0.3 volts and a minimum logic 1 of +2.4 volts applied to Pin 3 will lock the oscillator to the external source. The minimum sync pulsewidth should be 200 nanoseconds, and the maximum is determined by the required deadtime. The clock pin should never be driven more negative than -0.3 volts, nor more positive than +5.0 volts. The nominal resistance to ground is 3.2K at the clock pin, ±25% over temperature.

If two or more SG1524s must be synchronized together, program one master unit with R_T and C_T for the desired frequency. Leave the R_T pins on the slaves open, connect the C_T pins to the C_T of the master, and connect the clock pins to the clock pin of the master. Since C_T is a high-impedance node, this sync technique works best when all devices are close together.

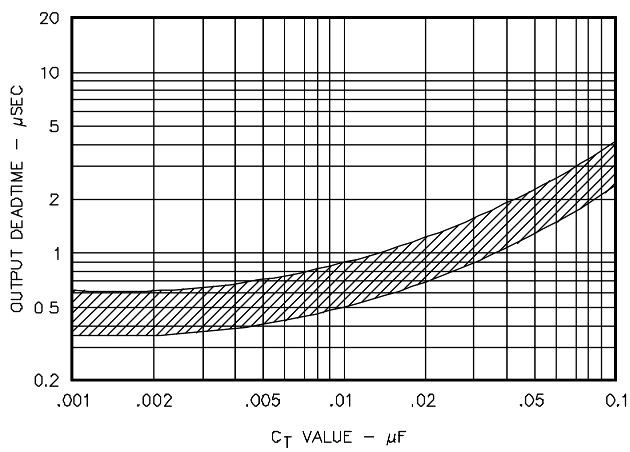


FIGURE 1 - OUTPUT STAGE DEADTIME VS. C_T

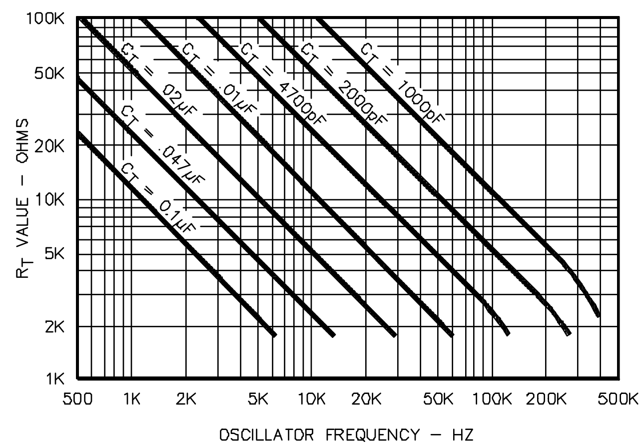


FIGURE 2 - OSCILLATOR FREQUENCY VS. R_T AND C_T

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APPLICATION NOTES (continued)

CURRENT LIMITING

The current limiting circuitry of the SG1524 is shown in Figure 3. By matching the base-emitter voltages of Q1 and Q2, and assuming a negligible voltage drop across R1:

$$\text{C.L. Threshold} = V_{BE}(Q1) + I_1 \bullet R_2 - V_{BE}(Q2) = I_1 \bullet R_2 \sim 200\text{ mV}$$

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use because of its simplicity.

The most important of these is the limited common-mode voltage range: ±0.3 volts around ground. This requires sensing in the ground or return line of the power supply. Also precautions should be taken to not turn on the parasitic substrate diode of the integrated circuit, even under transient conditions. A Schottky clamp diode at Pin 5 may be required in some configurations to achieve this.

A second factor to consider is that the response time is relatively slow. The current limit amplifier is internally compensated by R_1, C_1, and Q1, resulting in a roll-off pole at approximately 300 Hz. A third factor to consider is the bias current of the C.L. Sense pins. A constant current of approximately 150µA flows out of Pin 4, and a variable current with a range of 0-150µA flows out of Pin 5. As a result, the equivalent source impedance seen by the current sense pins should be less than 50 ohms to keep the threshold error less than 5%.

Since the gain of this circuit is relatively low (42 dB), there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage required to get 25% duty cycle (+2 volts at the error amplifier output) with the error amplifier signaling maximum duty cycle.

APPLICATION NOTE: If the current limit function is not used on the SG1524, the common-mode voltage range restriction requires both current sense pins to be grounded.

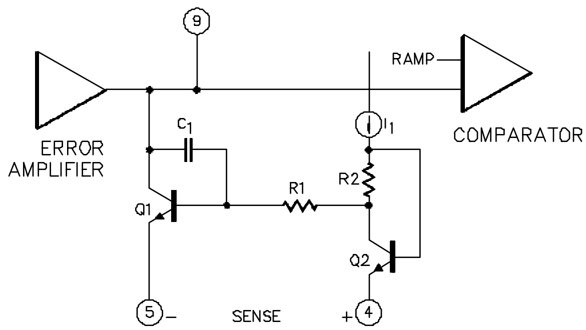
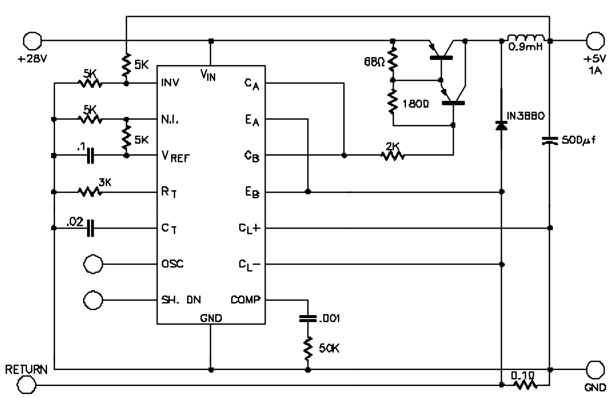
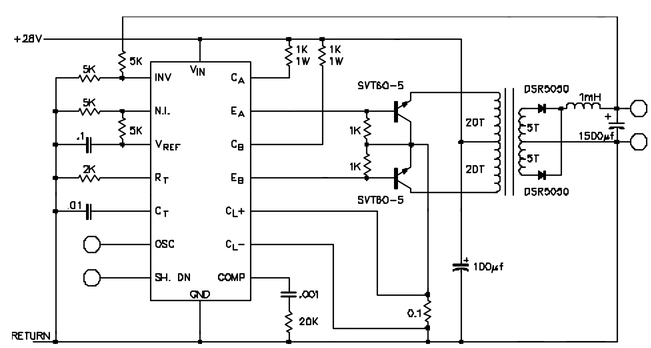


FIGURE 3 - CURRENT LIMITING CIRCUITRY OF THE SG1524



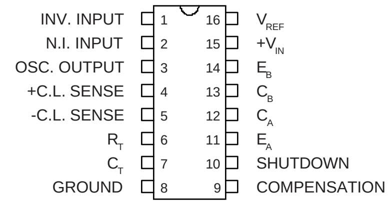
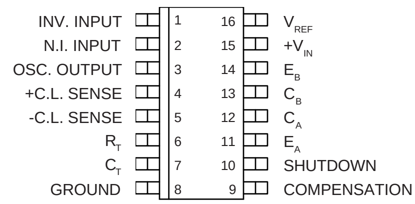
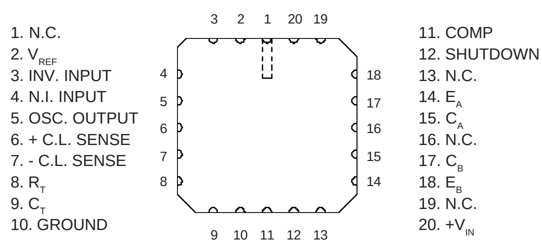
In this conventional single-ended regulator circuit, the two outputs of the SG1524 are connected in parallel for effective 0 - 90% duty-cycle modulation. The use of an output inductor requires and R-C phase compensation network for loop stability.



Push-pull outputs are used in this transformer-coupled DC-DC regulating converter. Note that the oscillator must be set at twice the desired output frequency as the SG1524's internal flip-flop divides the frequency by 2 as it switches the P.W.M. signal from one output to the other. Current limiting is done here in the primary so that the pulse width will be reduced should transformer saturation occur.

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CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

<table>
<tr><th>Package</th><th>Part No.</th><th>Ambient Temperature Range</th><th>Connection Diagram</th></tr>
<tr><td>16-PIN CERAMIC DIP
J - PACKAGE</td><td>SG1524J/883B
JAN1524J
SG1524J/DESC
SG1524J
SG2524J
SG3524J</td><td>-55°C to 125°C
-55°C to 125°C
-55°C to 125°C
-55°C to 125°C
-25°C to 85°C
0°C to 70°C</td><td rowspan="2">
</td></tr>
<tr><td>16-PIN PLASTIC DIP
N - PACKAGE</td><td>SG2524N
SG3524N</td><td>-25°C to 85°C
0°C to 70°C</td></tr>
<tr><td>16-PIN NARROW BODY
PLASTIC S.O.I.C.
D - PACKAGE</td><td>SG2524D
SG3524D</td><td>-25°C to 85°C
0°C to 70°C</td><td>
</td></tr>
<tr><td>20-PIN CERAMIC
LEADLESS CHIP CARRIER
L- PACKAGE</td><td>SG1524L/883B
SG1524L</td><td>-55°C to 125°C
-55°C to 125°C</td><td>
</td></tr>
</table>

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

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